An FPGA-based Accelerator for Sound Field Rendering with High-order FDTD

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(i) Introduction

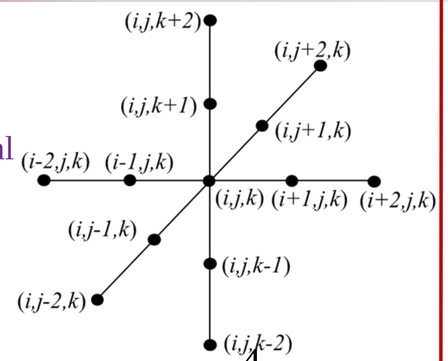
- FDTD is computation-intensive as the volume of sound space is increased because oversampling in spatial grids is required to suppress numerical dispersion.
- High-order FDTD is usually applied to reduce computation and memory requirement. In this research, an FPGA-based accelerator is developed to speed up computation in sound field rendering with the high-order FDTD scheme.

(ii) High-order FDTD Algorithm

$$\frac{\partial^2 P}{\partial t^2} = c^2\left(\frac{\partial^2 P}{\partial x^2} + \frac{\partial^2 P}{\partial y^2} + \frac{\partial^2 P}{\partial z^2}\right)$$

Second-order central difference method in time domain

Lagrange polynomial interpolation in spatial domain



High-order FDTD scheme

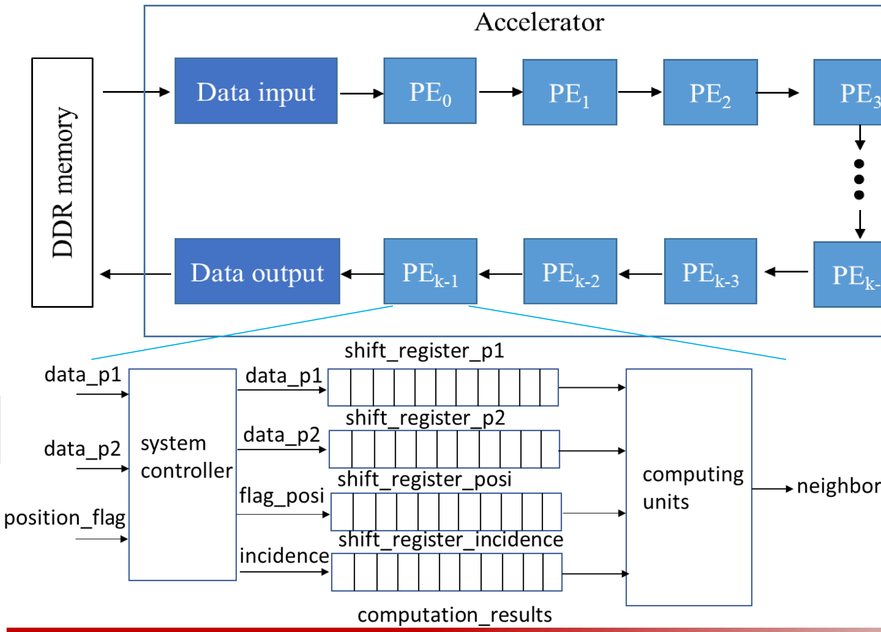
○ **4th-order scheme**

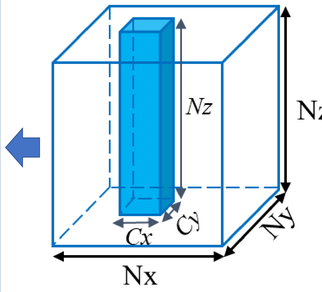
$$P^{n+1}_{i,j,k} = \chi^2[-\frac{1}{12}(P^n_{i-2,j,k} + P^n_{i+2,j,k} + P^n_{i,j-2,k} + P^n_{i,j+2,k} + P^n_{i,j,k-2} + P^n_{i,j,k+2}) + \frac{4}{3}(P^n_{i-1,j,k} + P^n_{i+1,j,k} + P^n_{i,j-1,k} + P^n_{i,j+1,k} + P^n_{i,j,k-1} + P^n_{i,j,k+1})] + (2 - \frac{15}{2}\chi^2)P^n_{i,j,k} - P^{n-1}_{i,j,k}$$

○ **6th-order scheme**

$$P^{n+1}_{i,j,k} = \chi^2[\frac{1}{90}(P^n_{i-3,j,k} + P^n_{i+3,j,k} + P^n_{i,j-3,k} + P^n_{i,j+3,k} + P^n_{i,j,k-3} + P^n_{i,j,k+3}) - \frac{3}{20}(P^n_{i-2,j,k} + P^n_{i+2,j,k} + P^n_{i,j-2,k} + P^n_{i,j+2,k} + P^n_{i,j,k-2} + P^n_{i,j,k+2}) + \frac{3}{2}(P^n_{i-1,j,k} + P^n_{i+1,j,k} + P^n_{i,j-1,k} + P^n_{i,j+1,k} + P^n_{i,j,k-1} + P^n_{i,j,k+1})] + (2 - \frac{49}{6}\chi^2)P^n_{i,j,k} - P^{n-1}_{i,j,k}$$

(iii) System Design





◆ System is designed using OpenCL. Spatial and temporal blockings are applied to speed up computation.

(iv) Performance Evaluation

➢ **Evaluation Environment:**

FPGA card: DE10-Pro.
FPGA: Stratix 10 SX (1SX280HU2F50E1VG)
# of DSP blocks: 5760
External DRAMs: 8 GB DDR4-2400
On-chip block RAMs: 28.6 MB
Clock frequency: about 350 MHz
Compiler: Intel FPGA SDK for OpenCL 19.1

Desktop for software simulation**:**
CPU: Intel Xeon Gold 6212U
# of Cores: 24
DRAMs: 512 GB DDR4-2933
Cache: L1:1.5 MB; L2: 24 MB; L3:35.75 MB
Clock frequency: 2.4 GHz
Cache: L1:1.5 MB; L2: 24 MB; L3:35.75 MB
Compiler: GNU compiler (gcc 4.8.5)

Others:
Sound space: 16m×8m×8m
Time steps: 32
Data: single precision
# of PEs: 16

Table 1. Hardware Resource Utilization

Orders	Logic Utilization	DSP Blocks	RAM Blocks	Frequency (MHz)
2nd	269,159 (29%)	342 (6%)	1,785 (15%)	357
4th	293001 (31%)	630 (11%)	3764 (32%)	355
6th	335,237 (36%)	918 (16%)	4,309 (37%)	337

Table 2 Rendering Time Per Time Step (s)

Orders	FPGA	Software Simulation
2nd	0.0486	0.5363 (11x)
4th	0.0333	0.4458 (13x)
6th	0.0238	0.4437 (18x)

(v) Acknowledgement

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