Performance Analysis of Applications under CPU Power Constraints

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Background and Purpose

With advancements in supercomputing, power consumption has surged, making energy a bottleneck that slows performance improvements. This has shifted research focus towards power-efficient hardware development and middleware optimizations, such as job scheduling. However, application-level power efficiency remains largely unexplored. As power constraints tighten, optimizing at the application level within a limited energy budget becomes crucial. Presently, analyses predominantly address performance metrics and projections, neglecting the impact of power limitations.

This study concentrates on enhancing power efficiency at the application level, evaluating supercomputer applications in the face of energy constraints. We explore the interplay between application performance metrics and power profiles and conduct a performance analysis for individual application segments.

Methodology

System

Configuration of subsystem B @Kyoto Univ

Dell EMC PowerEdge C6620		
node	CPU	Intel Xeon Platinum 8480+ (Sapphire Rapids) × 2
	Num. of core	56 cores /CPU
	Freq.	2.0 GHz (Turbo 3.8 GHz)
	L3	105 MB/CPU
	TDP	350 W
	Rpeak	7.2 TFlops (DP)
	Memory	DDR5 512 GB
	Bandwidth	614 GB/s
	B/F	0.085

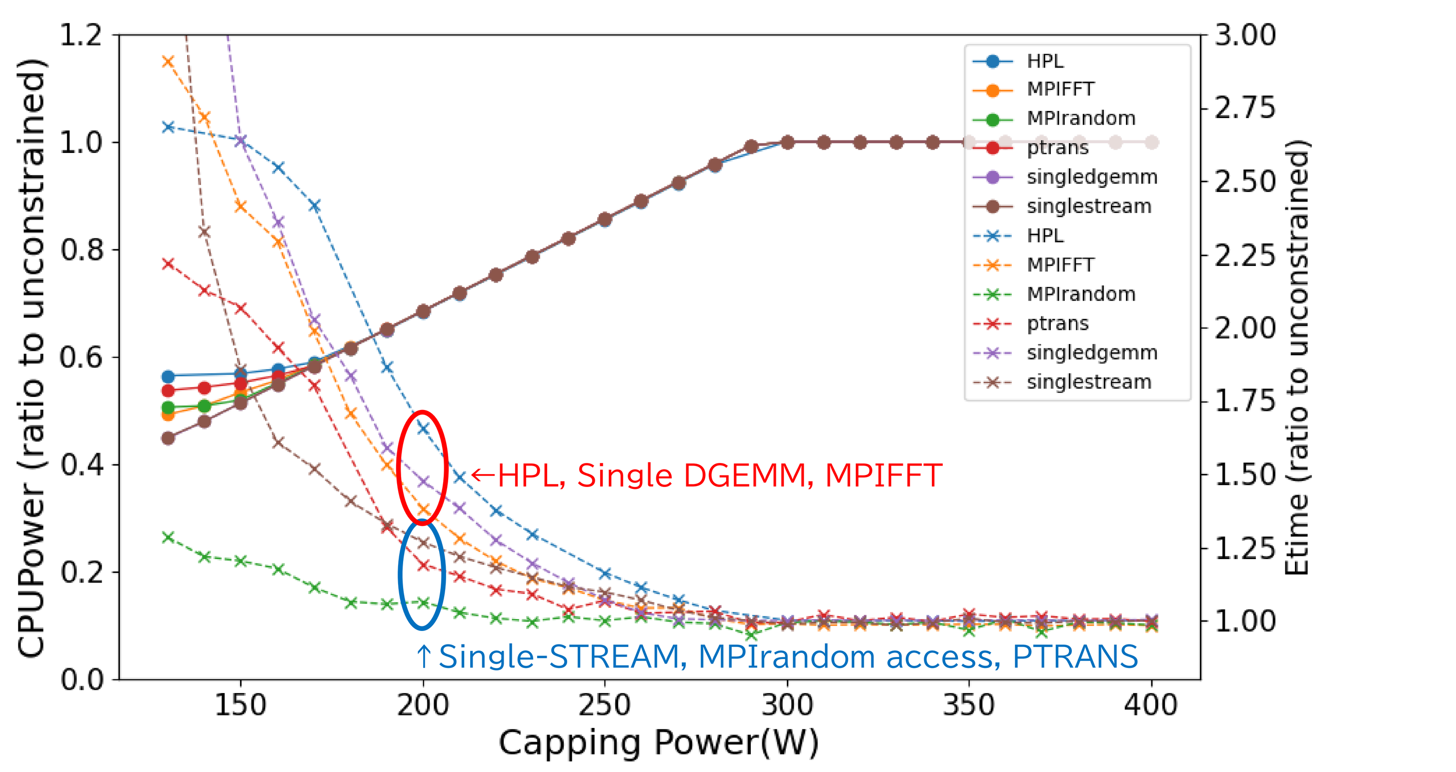
Note: This experiment is conducted on a single node

HPC Benchmarks and Applications

1. Single-DGEMM : Matrix multiplication program
2. Single-STREAM : Memory performance benchmark
3. HPL : LINPACK Benchmark
4. MPI-FFT : MPI parallelized Fast Fourier Transform benchmark
5. PTRANS : Communication performance benchmark through matrix transposition
6. MPI-RANDOM : Random memory access benchmark
7. poisson-omp : Thread-parallelized Poisson solver
8. poisson-mpi : Process-parallelized Poisson solver
9. pic-omp : Thread-parallelized in-cell particle method plasma simulation
10. pic-hybrid : Hybrid parallel OhHelp implemented in-cell particle method plasma simulation
11. fdtd-omp : Thread-parallelized space-time tiling FDTD simulation
12. fdtd-hybrid : Hybrid parallel space-time tiling FDTD simulation
13. fdtd-mpi : Process-parallelized space-time tiling FDTD simulation
14. mhd-single : Magnetohydrodynamics (MHD) simulation
15. mhd-sys : Array-optimized MHD simulation

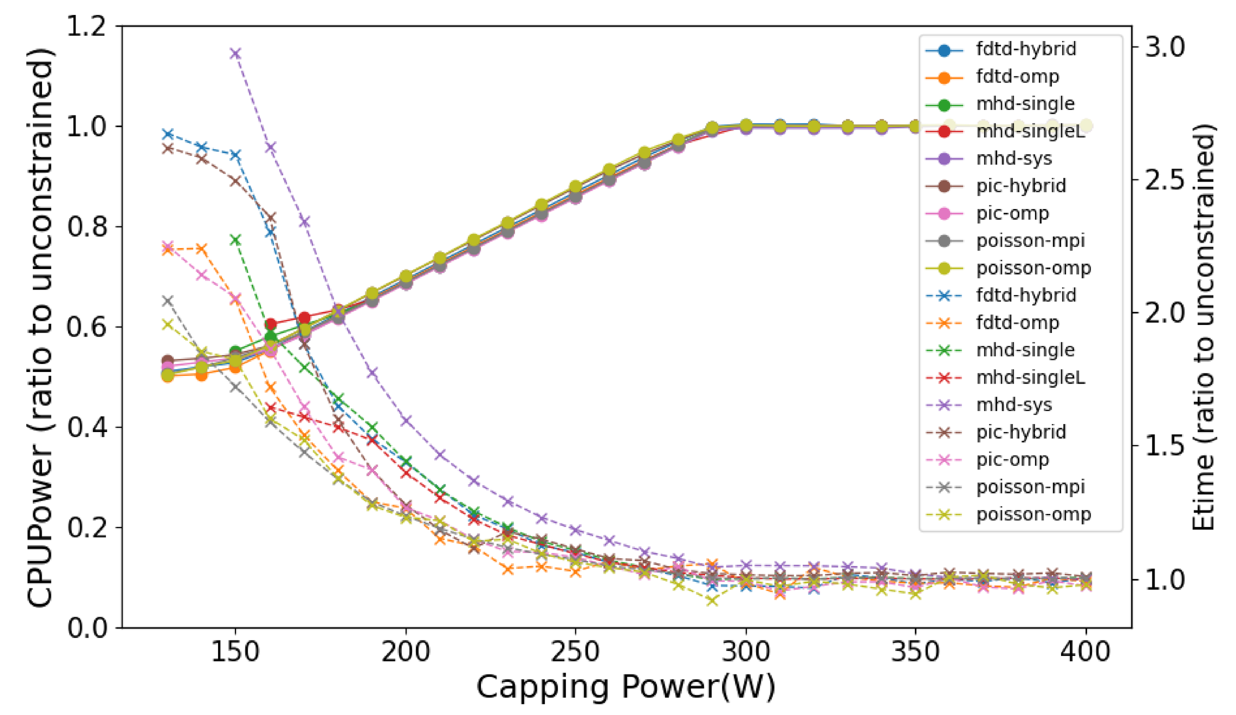
Results and Analysis

Overall performance evaluation of the HPCC benchmarks under CPU power constraints

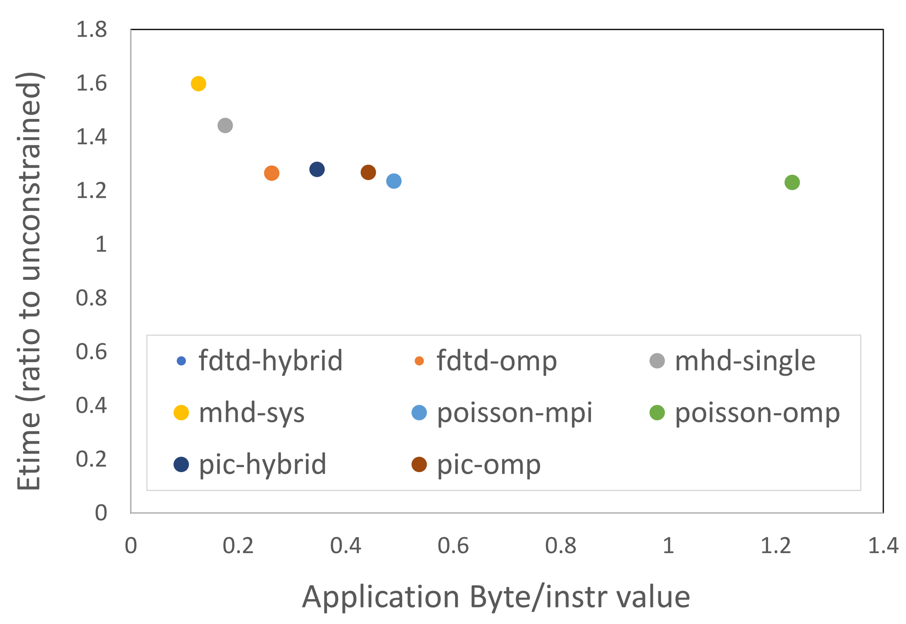


- Power consumption is equal until capping reaches 180W
- The top three sets with higher rates of increase in computation time are benchmarks related to computational speed, while the bottom three sets are related to communication speed

Overall performance evaluation of scientific applications and comparison with the required memory performance

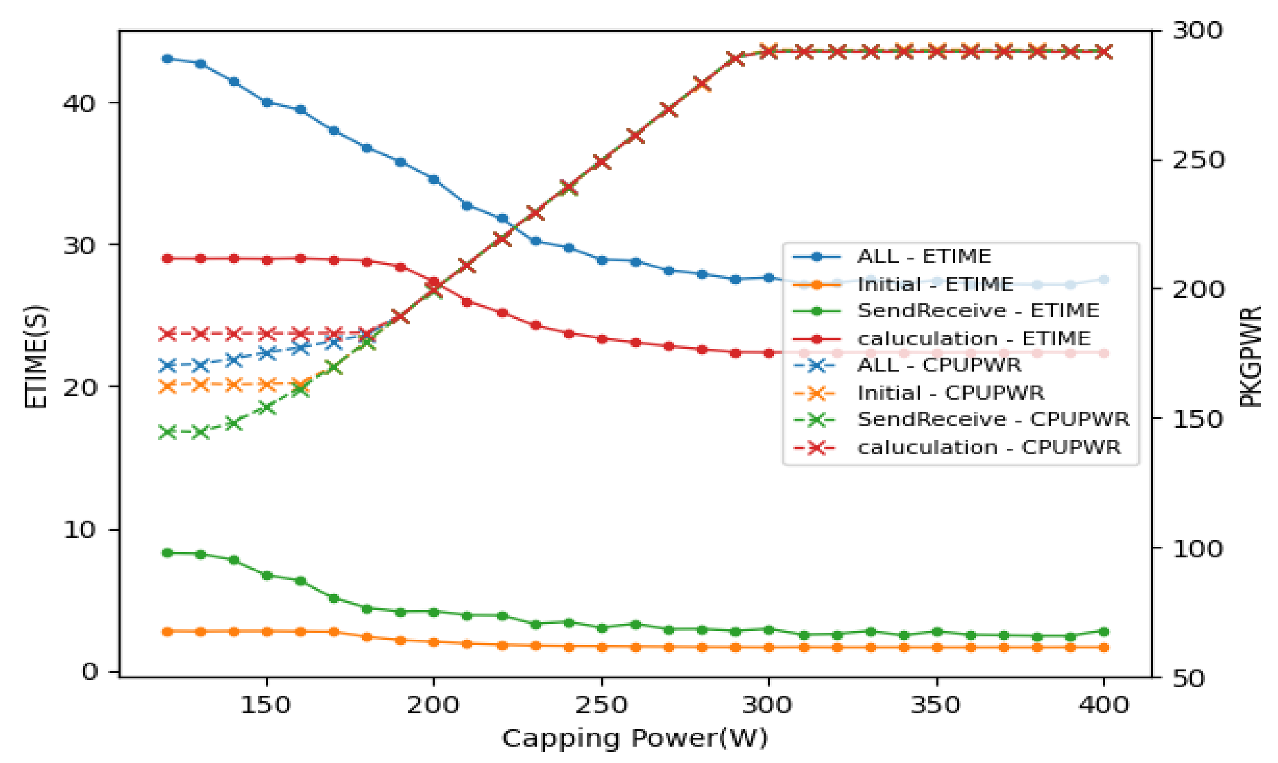


- Power consumption is equal until capping reaches 180W
- Performance begins to vary around 260W with Capping Power.



- The vertical axis represents computation time at 200W, and the horizontal axis represents the amount of memory access data required per instruction by the application
- Applications with low memory access data requirements per instruction (CPU-bound) are prone to degradation due to capping

Performance evaluation of each section within the fdtd-mpi application under CPU power constraints



- The main caluculation section begins to degrade quickly.
- The initialization section and inter-process communication are less prone to degradation

➡ **power capping for individual sections can result in power savings**

Conclusion and Future Work

- Evaluation of computational performance of HPC applications under CPU power constraints
  - Comparative evaluation of computational performance and application characteristic metrics
  - Evaluation by section of fdtd-mpi under CPU power constraints
    - power capping for individual sections can result in power savings
    - Evaluation by section of other scientific computing applications
- Power control for power saving based on the evaluation by section